

Fig 1

<u>Inst</u>	<u>Hit/Miss</u>	<u>Data</u>
18 — LDR [R <sub>m</sub> ]	Hit	Data [R <sub>m</sub> ]
MOV	N/A	—
CMP	N/A	—
⋮	⋮	⋮
20 — LDR [R <sub>m</sub> ]	Miss	—
MOV	N/A	—
CMP	N/A	Data [R <sub>m</sub> ]
⋮		
22 — LDR [R <sub>1</sub> ]	Miss	—
24 — LDR [R <sub>2</sub> ]	Miss	—
MOV	N/A	—
CMP	N/A	—
ADD	N/A	28 — Data [R <sub>2</sub> ]
		26 — Data [R <sub>1</sub> ]

variable delay

missed data returned out of order

Fig. 2

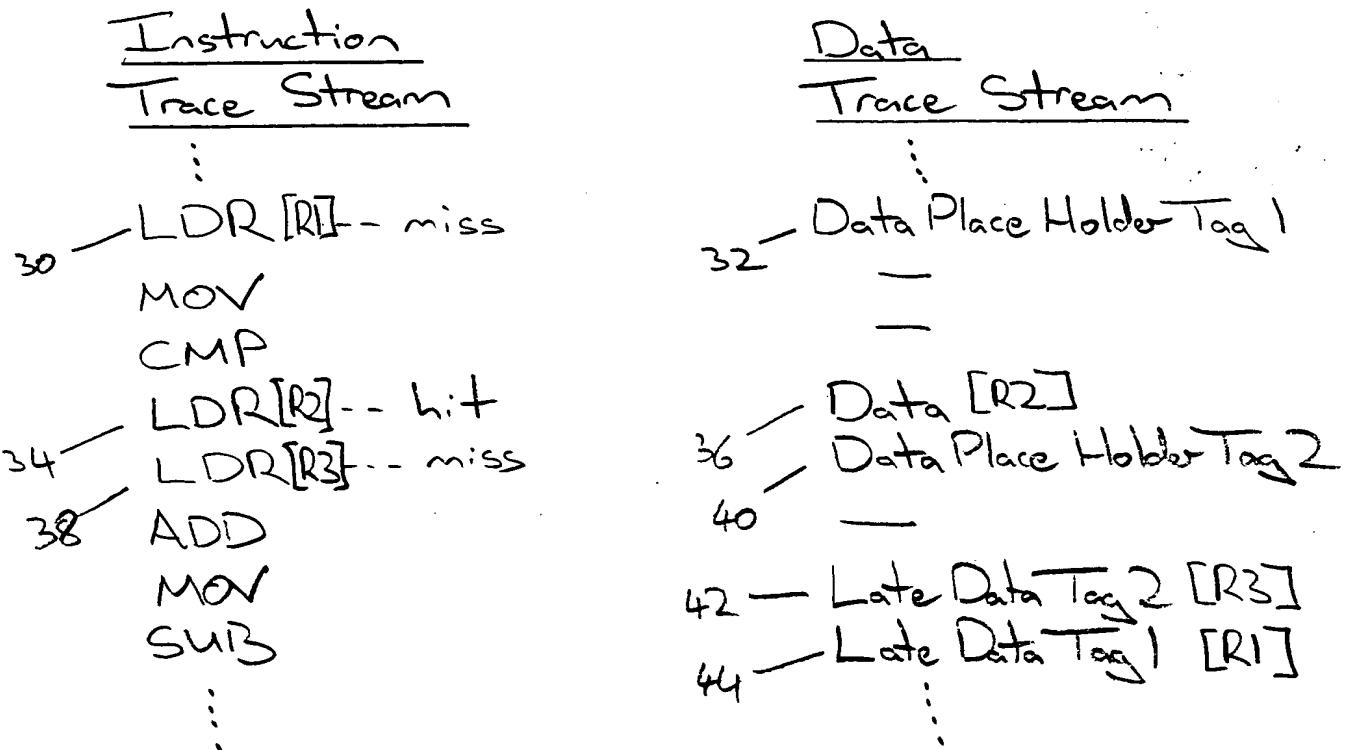


Fig. 3

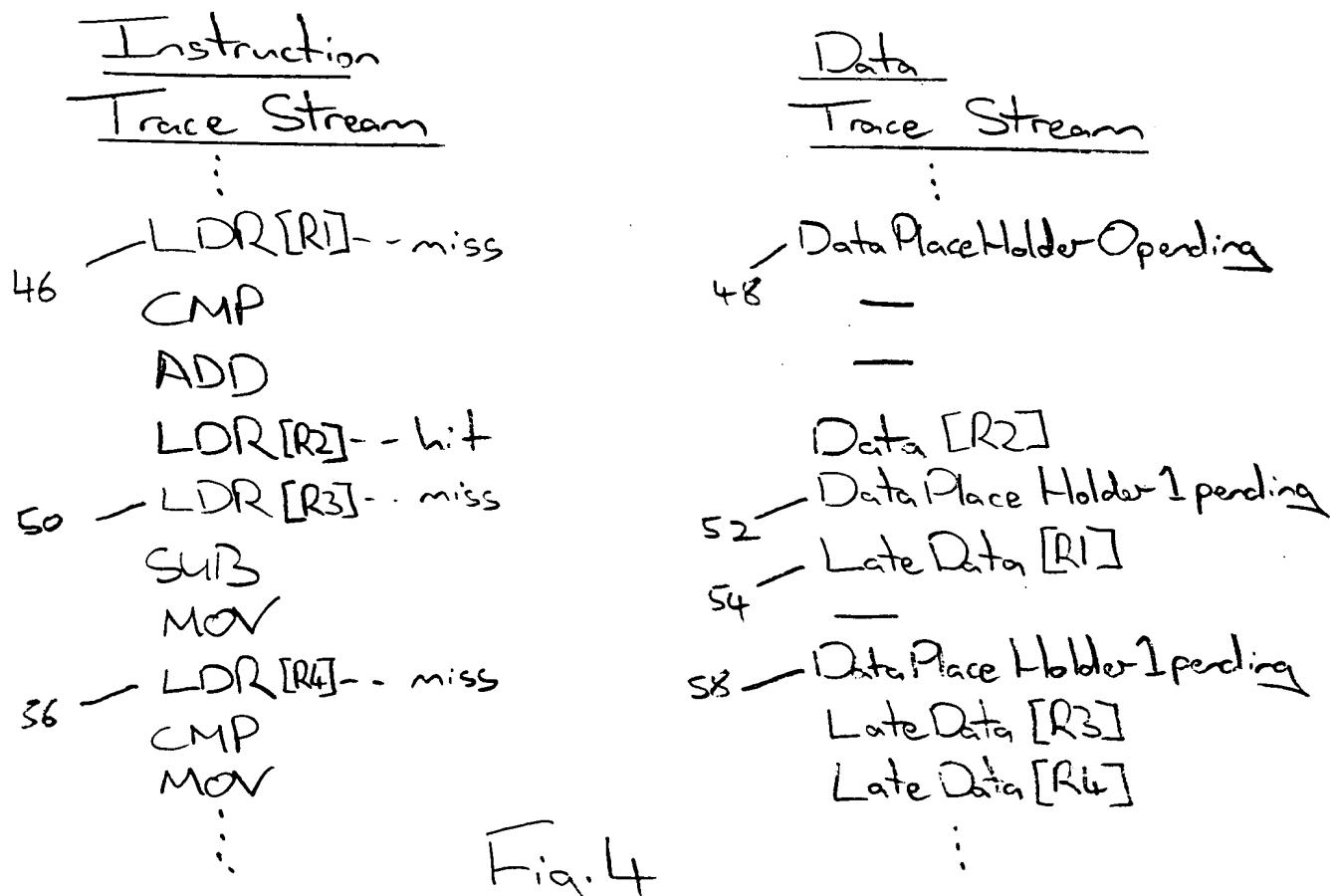


Fig. 4

Instruction Trace Stream

62 (LDR [R1] --- miss)  
 (MOV)  
 SUB  
 ↓  
 earliest trace info.  
 60 SYNC {1 pending}  
 LDR [R2] --- miss  
 CMP  
 ADD  
 64 LDR [R3] --- hit  
 MOV  
 SUB  
 CMP  
 .  
 .

Data Trace Stream

(Data Place Holder)  
 =  
 =  
 =

66 Data Place Holder  
 68 ~~LateData [R1]~~  
 =  
 Data [R3]  
 70 LateData [R2]  
 =  
 .

Fig. 5

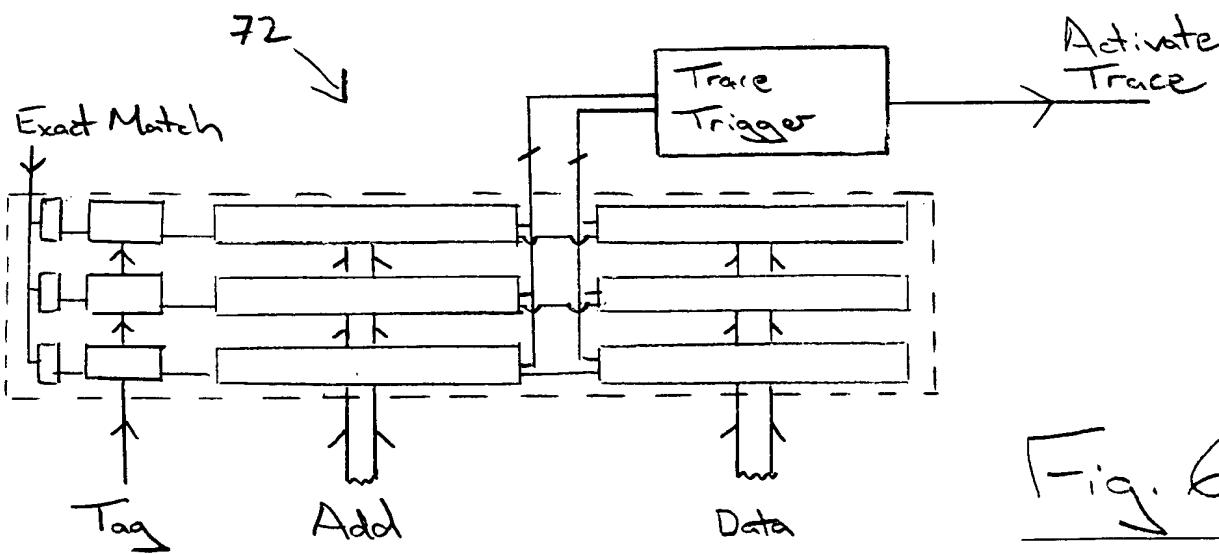


Fig. 6

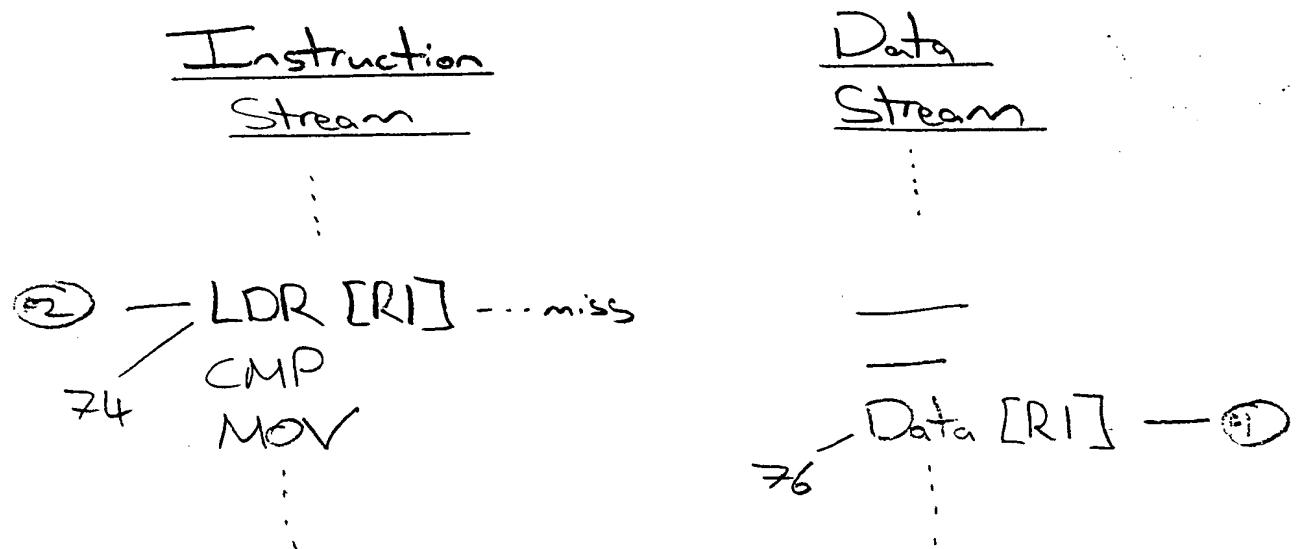
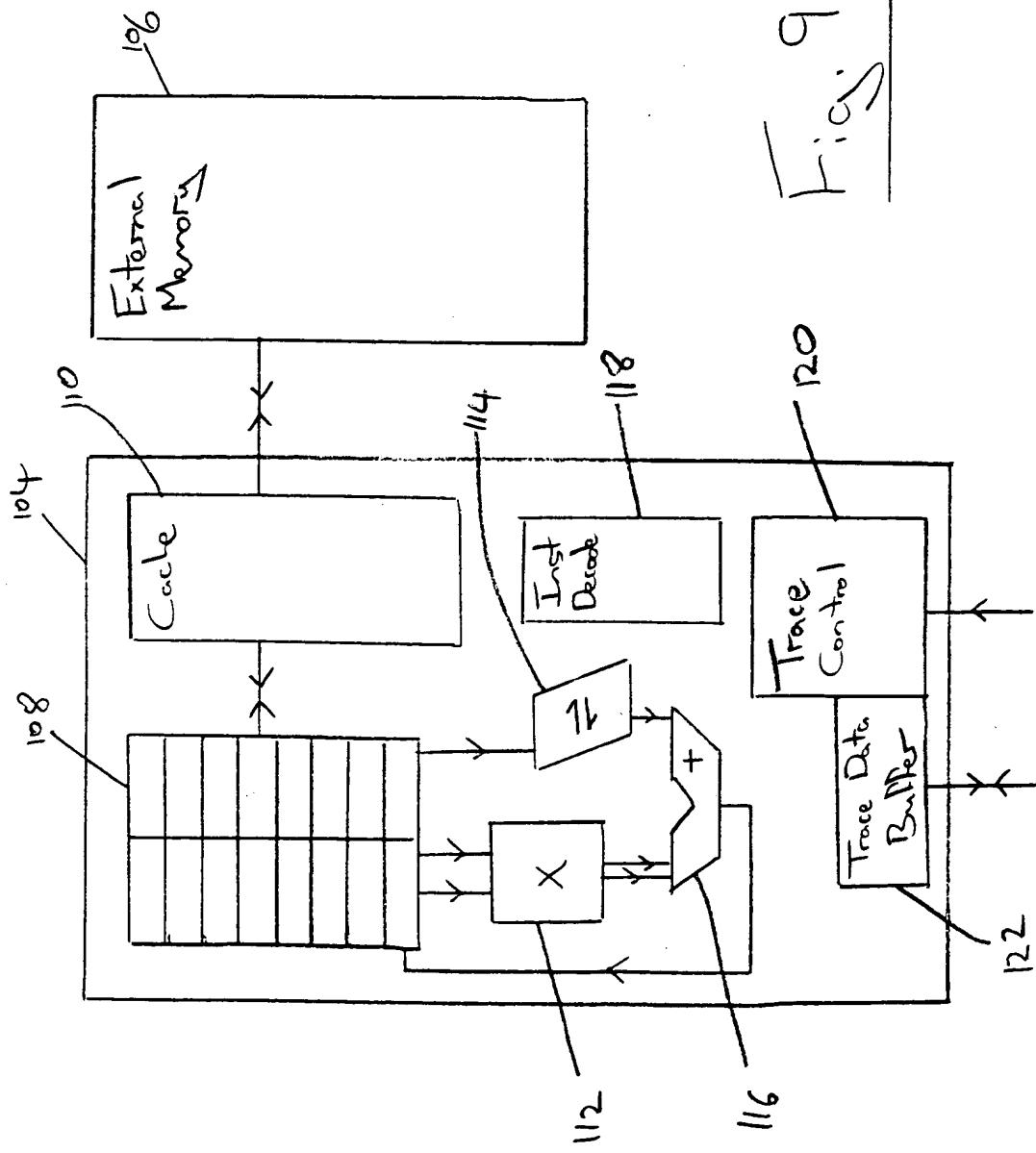


Fig. 7

Exact Match	Add Match	Data Match	Trace Activation Point
✓	✓	✓	①
✓	✓	✗	none
✗	✓	✓	②
✗	✓	✗	②

Fig. 8

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LSM  $R_n[\text{Add}], R_{\text{eq}}[\text{List}]$

16 bits

0000100010001000

⇓

$R_0$							
$R_1$							
$R_2$							
$R_3$							
$R_7$							
$R_{11}$							

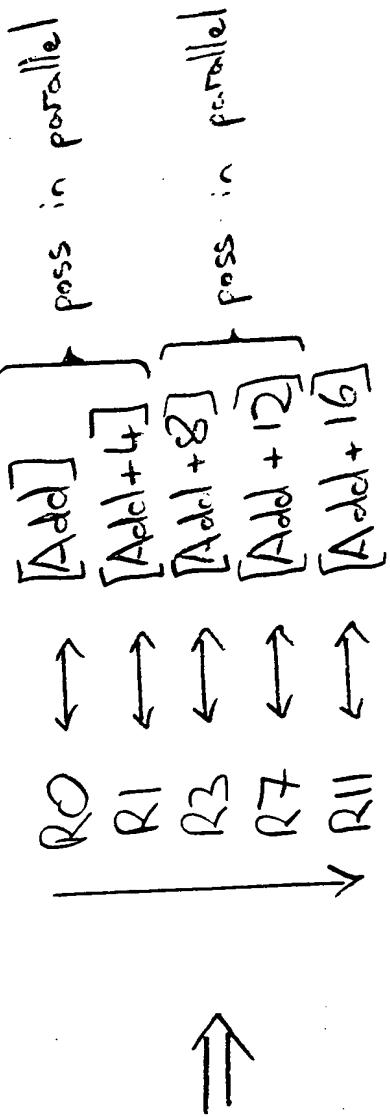


Fig. 10

$RO \xrightarrow{DW_1} [Add]$

$R1 \xrightarrow{DW_2} [Add+4]$

$R3^{\#} \xrightarrow{DW_3^*} [Add+8]$   
Trace Trigger

$R7 \xrightarrow{DW_4} [Add+12]$

Trace to End

$R11 \xrightarrow{DW_5} [Add+16]$



Trace Data Stream

$\{\{SM\}\}, \{DW_2\}, \{Add+8\}, \{PlaceHolder\}, \{PlaceHolder\}, \dots$

Log 11

Count back to R3

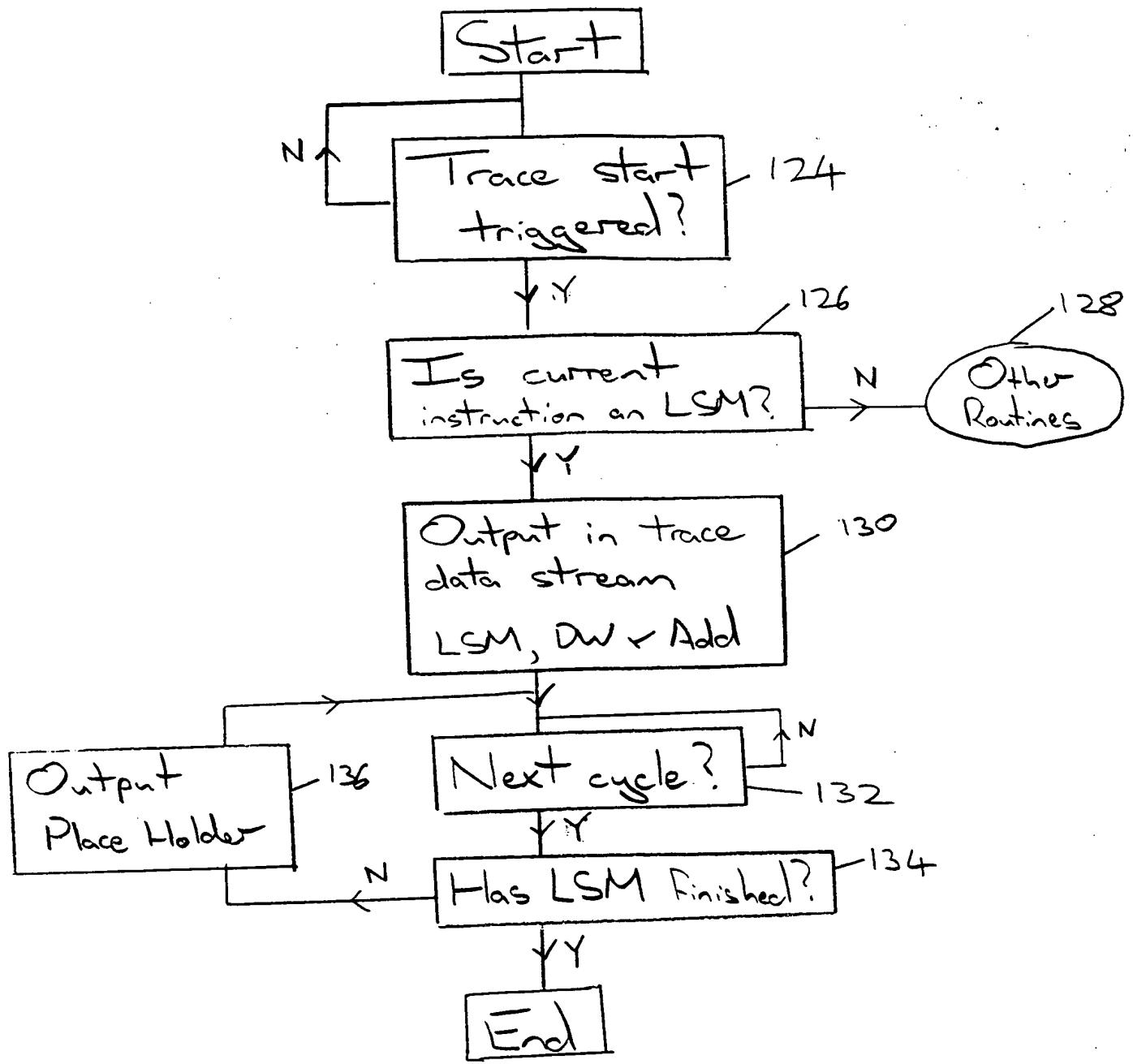


Fig. 12

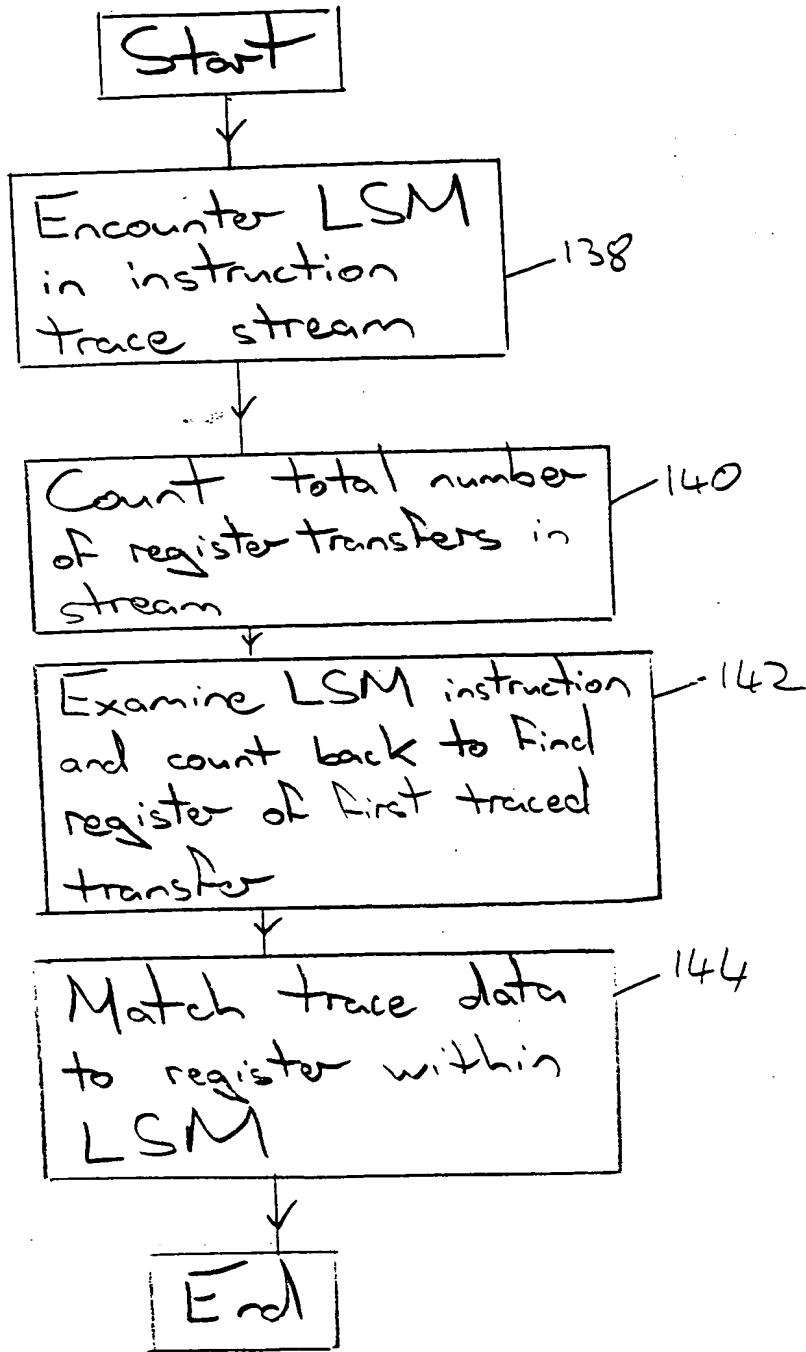


Fig. 13